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APPLICATION DATA SHEET

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TITLE: SYSTEM LEVEL BATTERY INTEGRATION SYSTEM

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SYSTEM LEVEL BATTERY INTEGRATION SYSTEM

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention generally relates to power supply units for electronic and computing systems, and more particularly to a system level power source integration to support handheld devices, computer systems, and other electronic equipment

Description of the Related Art

[0002] In today's wireless systems and personal systems continuous supply of power to maintain the quality of service becomes a major challenge. Using a battery to support the system usage becomes the primary operation mode in those systems. Although there are many new developments in the battery technology for longer usage period, lifetime, and operating environment, the integration of a battery into a system is proving to be bulky and inconvenient.

[0003] Currently, a battery management system is provided for very complex electrical and electronic-based circuits or devices, such as laptop computers, which typically utilize rechargeable batteries. In these applications, the battery management system typically provides a

specialized serial interface, such as the SMBus, for interfacing with an external controller such as a micro-controller. These battery management systems consist of specialized circuitry which is optimized for the unique chemistry of the specific battery type being monitored and controlled (i.e., nickel cadmium, lithium, etc.).

[0004] A number of advanced battery technologies have recently been developed, such as metal hydride (e.g., Ni-MH), lithium-ion, and lithium polymer cell technologies, which would appear to provide the requisite level of energy production and safety margins for many commercial and consumer applications. However, such advanced battery technologies often exhibit characteristics that provide challenges for the designers and manufacturers of advanced energy storage devices.

[0005] Moreover, in recent years, there has been accelerated development of down-sized and cordless design schemes in the field of electronics apparatus or equipment. In view of this trend, batteries and battery systems are of increasing interest since these have increased applicability as the power supply for such electronic equipment due to their capability of size reduction and high electrical energy density.

[0006] These battery management systems and the associated microcontroller utilize current or voltage level monitoring techniques to switch between battery sources and/or to shut down the device being powered at a battery discharge level that is controlled by data stored in the memory. As such, current battery management systems are vastly complex and cost significantly greater than what can be justified for cheaper devices.

[0007] Additionally, the demand for new and improved electronic and electro-mechanical systems have placed increased pressure on the designers and manufacturers of energy storage

devices to develop battery technologies that provide for high energy generation in a low-volume package. Conventional battery systems, such as those that utilize lead acid for example, are often unsuitable for use in high-power, low-weight applications. Other known battery technologies may be considered too unstable or hazardous for use in consumer product applications, such as portable wireless devices.

[0008] In accordance with a conventional advanced battery design, individual cells are hardwired together and to the positive and negative power terminals of the battery. Various electronic components which may be incorporated into the battery design must also be hardwired to the cells. It should be apparent to those skilled in the art that such conventional interconnection approaches provide for little, if any, flexibility when attempting to alter the series and/or parallel hardwired connections between the cells and components.

[0009] Moreover, the wiring process typically employed in the fabrication of conventional advanced batteries is generally complicated and time consuming. Of particular concern to the designers and manufacturers of conventional advanced batteries are the unintentional wiring shorts, which develop during the wiring process. These and other design defects typically result in a reduction in the performance and service life of the battery, and often represent a significant safety concern.

[0010] Other characteristics of advanced battery technologies provide additional challenges for the designers of advanced energy storage devices. For example, certain advanced cell structures are subject to cyclical changes in volume as a consequence of variations in the state of charge of the cell. The total volume of such a cell may vary as much as five to six percent during charge and discharge cycling. Such repetitive changes in the physical size of a cell

significantly complicates the mechanical housing design and electrical connection strategy. The electrochemical, thermal, and mechanical characteristics of an advanced battery cell must typically be well understood and appropriately considered when designing an energy storage system suitable for use in commercial and consumer devices and systems.

[0011] However, there remains a need for an integrated solution of chips and packaging as a new concept for the power source at the chip packaging and system level. Moreover, there is a need for a system level self-powered system, which provides flexibility and reliability, and which can be manufactured easily and at a lower cost than conventional systems.

SUMMARY OF THE INVENTION

[0012] In view of the foregoing and other problems, disadvantages, and drawbacks of the conventional power source system units the present invention has been devised, and it is an object of the present invention to provide a structure and method for an integrated solution of chips and packaging as a new concept for the power source at the chip packaging and system level.

[0013] It is another object of the present invention to provide a packaging and system level battery solution for the System On Chip (SOC) chip level packaging and portable system levels.

[0014] Yet another object of the present invention is to provide technology, which can be the sole power source for smaller and lower power systems and the supplementary power for higher power systems.

[0015] In order to attain the objects suggested above, there is provided, according to one aspect of the invention a method and structure for a system level integration of a solid state battery, or other types of batteries, with an integrated circuit chip comprising a battery, an integrated circuit chip powered by the battery, and a package connected to the battery and the integrated circuit chip. The package connects to the integrated circuit chip through an interior portion of the package, and the battery overhangs the integrated circuit chip, wherein the integrated circuit chip connects to an upper indent portion of the package, and wherein the battery is larger than the integrated circuit chip. Alternatively, the solid state battery connects to an underside of the package. Additionally, there may be a stack of batteries used, or multiple integrated circuit chips arranged in a multi-chip module.

[0016] There are numerous benefits of the integration of chips and a battery, according to the present invention. For example, the present invention greatly reduces the overall system size. Second, the present invention improves the power supply efficiency, since the battery chip is located very close to the system. Hence, the energy waste due to resistive loss caused by having a power supply through a long resistive power bus, is eliminated. Another advantage is that power management becomes easier, since the battery chip includes battery cell arrays in addition to relevant control circuitry. Yet another benefit is the noise due to the power supply is reduced by reducing the wire inductance. Moreover, the present invention allows for decoupling capacitors and regulators to be added, which can also be integrated on the battery chip to manage the noise. Still another advantage of the present invention is that the thermal effect caused by the battery charging and discharging is minimized. Along these lines, by reducing battery heat-up during charging, the battery life span is increased, and the charging efficiency is greatly improved.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] The foregoing and other objects, aspects and advantages will be better understood from the following detailed description of the preferred embodiments of the invention with reference to the drawings, in which:

[0018] Figure 1 is a schematic diagram of a first embodiment of an integrated battery and chip packaging system;

[0019] Figure 2(a) is a schematic diagram of a second embodiment of a battery and chip packaging system;

[0020] Figure 2(b) is a schematic diagram of a third embodiment of a battery and chip packaging system;

[0021] Figure 2(c) is a schematic diagram of a fourth embodiment of a battery and chip packaging system;

[0022] Figure 3 is a schematic diagram of a fifth embodiment of a battery and chip packaging system illustrating a sub-system level integration of a battery system; and

[0023] Figure 4 is a flow diagram illustrating a preferred method of the invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS OF THE INVENTION

[0024] As previously mentioned, there is a need for an integrated solution of chips and packaging as a new concept for the power source at the chip packaging and system level, and for

a system level self-powered system, which provides flexibility and reliability, and which can be manufactured easily and at a lower cost than conventional systems. The invention addresses these needs by providing solutions of on-chip solid-state battery technology and power system for on-chip batteries. The present invention further provides for the integration of other battery types (other than solid-state batteries). The present invention uses packaging technology, wherein the solid-state battery can be fabricated independently and packaged to the chip or package.

[0025] Referring now to the drawings, and more particularly to Figures 1 through 4, there are shown preferred embodiments of the method and structures according to the present invention. In Figure 1, a schematic diagram of a first embodiment of an integrated solid-state battery and chip packaging system 100 is illustrated with a solid-state battery 102 shown on a finished chip 101. The solid-state battery chip (e.g., capacitor, etc.) 102 is soldered to the underside of a chip further comprising an integrated circuit 101. The battery electrodes 103 can be soldered to the chip through a micro-C4 or similar technique to the chip voltage sources. Then the entire stacked chips can be placed into a standard package 104. Since the battery chip 102 is placed in the middle of the chip 101, this structure is more ideal for the chip having low number of input and output (I/O) pins 103 and does not require a full chip size battery. To add extra power capability, a larger size battery is usually required.

[0026] The advantages of this embodiment are that the battery is directly attached to the silicon chip by using soldering techniques. Moreover, this embodiment produces the lowest resistance and inductance between the battery terminals and chip power supply pads, thus the noise generated by inductance is minimized and the resistance loss of the power supply current is minimized. The shaded area 105 between the chip 101 and the packaging 104 is the backside

attachment of the chip 101, which can be either conductive or non-conductive. The two wires 106a, 106b are the wires bonded to the bonding pads (not shown) on the chip periphery 101. Since the chip 101 is placed facing upward, the on-chip battery 102 covers the center of the chip 101. Moreover, the input/output pads 103 are connected to the packaging through the wires 106a, 106b.

[0027] In Figures 2(a) through 2(c) several other embodiments are shown. As such, several methods exist to place the battery into the chip package as an integrated part of the chip packaging. In Figure 2(a) a solid-state battery 220 with a size larger than the integrated circuit chip 210 is placed over the rim of the package 240 with power supply and ground electrodes 230 contacting the package 240 directly.

[0028] In this second embodiment, the chip packaging is the same as the regular packaging method. There are several soldering bumps 250 for the silicon chip input and output pins. Some of the I/O pins are power/ground pins. The connections 250 to the chip 210 are through the packaging interior 240. The battery power and ground are fed through the packaging structure to the power/ground pins. Although, this structure has a reduced resistance and inductance compared to a conventional system, it has a slightly higher resistance and inductance compared to the first embodiment since the power and ground wires are of finite length in the packaging. However, for chips with a large number of I/O, such as microprocessors, this is a preferred embodiment because there is no blockage from the battery. The embodiment shown in Figure 2(a) is different from the embodiment shown in Figure 1 in that the chip 210 is facing downward and connected to the packaging 240 through soldering balls 250. Here, the battery

220 is behind the chip 210 and can only be connected to the chip power electrodes 230 through the packaging 240.

[0029] In Figure 2(b), a third embodiment illustrating a different mode of packaging is shown, wherein the solid-state battery 220 is placed over the opposite side of the packaging 240 with power supply and ground electrodes 230 contacting the package 240 directly. The connections 250 to the chip 210 are through the packaging interior 240. This embodiment provides a better connection between the battery electrodes to the packaging in comparison to the second embodiment shown in Figure 2(a). In the second embodiment, the battery to packaging connection is alone in the rim of the package, which can increase the path of the power and ground lines. Also, the size of the contacts between the battery and package is limited by the width of the rim. Conversely, in this third embodiment, the connection wire from the battery can be fed through the package and connect to the chip.

[0030] In Figure 2(c), a fourth embodiment of packaging is disclosed. Here, the package is similar to the second embodiment shown in Figure 2(a). However, in the fourth embodiment, several solid-state batteries 220 are stacked to increase the capacity and prolong the usage period. Using a larger battery instead of several stacked batteries can also be suitable if the solid-state battery can be fabricated into the multi-level structure. The solid-state battery is based on the area of cells with temperature and charge/discharge control circuit. Usually, it is fabricated in a thin layer form. However, a large battery with several layers can also be used. Because these solid-state batteries 220 are connected to each other through a low temperature soldering technique, the number of batteries in the stack is flexible. The biggest advantage of the fourth embodiment is the increase in battery lifetime and reduction of the resistance/inductance inside the packaging.

[0031] In Figure 3, a fifth embodiment is shown, wherein a sub-system 300 is disclosed with several chips 320 packaged in a multi-chip-module (MCM) 340. The chips 320 are powered by a large full MCM size solid-state battery 310. The battery 310 becomes the power source for the entire system. The sub-system 300 may content several chips 320 as part of the complete system 300. Moreover, the packaging can be a MCM type of structure. A larger size battery is preferably used, but is not necessary. Rather, the choice depends on the type of chips in this system and the power consumption of these chips. This embodiment constitutes the preferred embodiment of the present invention. In a conventional system, the MCM, which contains several chips to form a sub-system, must be packaged to a board to get power. Thus, in the conventional systems, the benefit of data and signal integration is not available to the supply lines.

[0032] Therefore, in the preferred embodiment, the size of the system is reduced because of the elimination of a large number of wires in the packaging levels; instead the wires are in the MCM level. Moreover, the noise, power, and speed are greatly improved. Also, in the preferred embodiment, the battery 310 is included into the MCM module 340 to integrate the power supply into the sub-system 300. This integrated system 300 can be operated by itself as a small system, for example, such as a cellular phone, PDA, etc., or combined with other components within a large system. Furthermore, the battery 310 within the sub-system 300 can serve as a backup power supply to preserve the data and processing activity during power down mode. The preferred embodiment is convenient for smaller systems such as a wireless handset, personal systems, and digital player machines.

[0033] The advantages of the integration of chips and a battery (chip), according to the present invention, are several. For example, the present invention greatly reduces the overall

system size. Second, the present invention improves the power supply efficiency, since the battery chip is located very close to the system. Hence, the energy waste due to loss and thermal dissipation, caused by having a power supply through a long resistive power bus, is eliminated. Another advantage is that power management becomes easier, since the battery chip includes battery cell arrays in addition to relevant control circuitry.

[0034] Yet another benefit is the noise, due to the power supply, is reduced. Moreover, the present invention allows for decoupling capacitors and regulators to be added, which can also be integrated on the battery chip to manage the noise. Still another advantage of the present invention is that the thermal effect caused by the battery charging and discharging is minimized The thermal effect is minimized by integrating the battery controller and voltage regulator into the packaging instead of using an external chip. Moreover, the temperature control to operate the battery is more efficient. Along these lines, by reducing battery heat-up during charging, the battery life span is increased, and the charging efficiency is greatly improved.

[0035] Figure 4 depicts a flow diagram illustrating a preferred method of the invention comprising the steps of connecting 400 at least one integrated circuit chip 210, 320 to a package 240 or a multi-chip module 340. Next, the at least one solid state battery 220, 310 is connected 410 to the package 240 or the multi-chip module 340. Finally, the at least one integrated circuit chip 210, 320 is powered 420 by the at least one solid state battery 220, 310.

[0036] While the invention has been described in terms of preferred embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims.